REMARKS

Reconsideration and re-examination are hereby requested.

Before discussing the claims and how they distinguish over the cited art, perhaps it might be helpful to review features of applicant's invention.

Reference is made to page 23, beginning at line 22:

> As described above in connection with Step 510, the CPU 310 generates a destination vector indicating the **director, or directors**, which are to receive the message. As also indicated above the command field is 32-bytes, eight bytes thereof having a bit representing a corresponding one of the 64 directors to receive the message. For example, referring to FIG. 11C, each of the bit positions 1-64 represents directors 180_1-180_{32}, 200_1-200_{31}, respectively. Here, in this example, because a logic 1 is only in bit position 1, the eight-byte vector indicates that the destination director is only front-end director 108_1. In the example in FIG. 11D, because a logic 1 is only in bit position 2, the eight-byte vector indicates that the destination director is only front-end director 108_2. In the example in FIG. 11E, because a logic 1 is more than one bit position, the destination for the message is to more than one director, i.e., a multi-cast message. In the example in FIG. 11E, a logic 1 is only in bit positions 2, 3, 63 and 64. Thus, the eight-byte vector indicates that the destination directors are only front-end director 108_2 and 180_3 and back-end directors 200_{31} and 200_{32}. There is a mask vector stored in a register of register section 420 (FIG. 7) in the message engine (ME) 315 which identifies director or directors which may be not available to use (e.g. a defective director or a director not in the system at that time), Step 524, 525, for a uni-cast transmission). If the message engine (ME) 315 state machine 410 indicates that the director is available by examining the transmit vector mask (FIG. 11F) stored in register 420, the message engine (ME) 315 encapsulates the message payload with a MAC header and CRC inside the packetizer portion 428P, discussed above (Step 526). ***An example of the mask is shown in FIG. 11F. The mask has 64 bit positions, one for each one of the directors. Thus, as with the destination vectors described above in connection with FIGS. 11C-11E, bit positions 1-64 represents directors 180_1-180_{32}, 200_1-200_{32}, respectively. Here in this example, a logic 1 in a bit position in the mask indicates that the representative director is available and a logic 0 in such bit position indicates that the representative director is not available. Here, in the example shown in FIG. 11F, only director 200_{32} is unavailable. Thus, if the message has a destination vector as indicated in FIG. 11E, the destination vector, after passing through the mask of FIG. 11F modifies the destination vector to that shown in FIG. 11G. Thus, director 200_{32} will not receive the message. Such mask modification to the destination vector is important because, as will be described, the messages on a multi-cast are sent sequentially and not in parallel. Thus, elimination***

of message transmission to an unavailable director or directors increases the message transmission efficiency of the system. (Emphasis added)

Referring now to the Baum et al. (U. S. Patent No. 5,166,674), the Examiner refers to Figure 11 and column 11, lines 50-68 and column 12, lines 1-51. These sections are presented below for convenience:

> The command field (CMD) includes a five bit command that tells the cluster controller and the receiving processing element how to handle the packet. The sequence number field (SEQ) includes an 8 bit packet sequence number sequentially assigned by the originating (source) processing element. The sequence number enables the receiving system to identify which packet number of the total packet count in the message has been received.
>
> The destination address field (DST) includes a fifteen bit destination processing element number. The destination field is used by the switch and cluster controller to self route the packet and by the receiving (destination) processing element to verify that the packet has been routed to the proper address.
>
> The source address field (SRC) includes a fifteen bit originating (source) processing element number. The source field is used by the switch and cluster controller to return the packet to the source in a case where an inoperable or non-present processing element number appears in the destination address field (DST) field, and by the receiving (destination) processing element to properly address any response to the message or command.
>
> The data field (DATA) includes 128 bits of information. The type of information in the data field is defined by the command field (CMD).
>
> The ECC Field (ECC) includes an SEC/DED (Single Error Correct/Double Error Detect) error correction code.
>
> For message header packets, the sequence field specifies the total length of the message, and the DMA controller allocates a message buffer of this length in the PE local memory, writes the initial quadword of data into the message buffer, and sets local hardware pointer, length and sequence registers if there will be more packets of data for this message. It also constructs the message header in memory, which includes the message length, DST id and SRC id.
>
> For message body packets, the sequence number field is checked against the sequence register to verify that packets are arriving in order, and each quadword of data is added to the message buffer. When the message has been completely received it is enqueued on a queue in local memory, known as the IN_QUEUE, for processing by the local processor. If the IN_QUEUE had been

empty prior to the addition of this message, then an interruption is generated to the local processor to notify it of pending work.

For storage access command packets, the DMA controller performs the required fetch or store operation to the PE local memory (transferring a doubleword of data), and for fetches a response packet is constructed by reversing the SRC and DST id fields, and then sent on the through the switch to return the requested doubleword of data.

Packets that contain global storage access commands are handled in the cluster controller in the same way that local storage access commands are handled by the DMA controllers. In both cases, the memory operations are autonomous, and include a compare-and-swap capability.

It is respectfully submitted that the sections in Baum et al., referred to above, provide no description or suggestion of the any one of the following features set forth the claims, below:

Claim 1 points out that:

such descriptor having a command field indicating the one or ones of the directors which are to receive such message, such command field having a plurality of bits, each bit being associated with a corresponding one of the directors, one logic state of such bit indicating that such corresponding director is to receive the message and another logic state of such bit indicating that such corresponding director is not to receive such message

It is respectfully submitted that such feature is not described or suggested in Baum et al.

Claim 5 points out that:

such command field having a plurality of bits, each bit being associated with a corresponding one of the directors, one logic state of such bit indicating that such corresponding director is to receive the message and another logic state of such bit indicating that such corresponding director is not to receive such message.

It is respectfully submitted that such feature is not described or suggested in Baum et al.

Claim 9 points out that :

each bit being associated with a corresponding one of the directors, one logic state of such bit indicating that such corresponding director is to receive the message and another logic state of such bit indicating that such corresponding director is not to receive such message.

It is respectfully submitted that such feature is not described or suggested in Baum et al.

Claim 13 points out that:

such descriptor having a command field indicating the one or ones of the directors which are to receive such message, such command field having a plurality of bits, each bit being associated with a corresponding one of the directors, one logic state of such bit indicating that such corresponding director is to receive the message and another logic state of such bit indicating that such corresponding director is not to receive such message.

In view of the foregoing, it is applicant's position that the claims are patentable over Baum et al.

With regard to the provisional double patenting rejection, the Examiner states that "a 'command field' would have been obvious to be included in the system interface in order to indicate whether the directors receive the message or not" and the Examiner refers to Baum et al. discussed above. It is respectfully submitted that such conclusion is not supported by Baum et al. because Baum et al, for the reasons set forth above, makes no such suggestion.

Please charge any cost incurred in the filing of this Amendment, along with any other costs, to Deposit Account 50-0845.

Respectfully submitted,

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